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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,076	10/04/2003	Paul E. McKenney	BEA920030004US1	3528

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EXAMINER	
BERTRAM, RYAN	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,076	MCKENNEY ET AL.	
	Examiner	Art Unit	
	RYAN BERTRAM	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 6/25/2008. At this point claim 1 has been amended and claims 12-20 have been cancelled. Thus, claims 1-11 are pending in the instant application.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajwar et al. (US 7,120,762) hereinafter Rajwar.

1. Regarding claim 1, Rajwar teaches a method comprising:

executing a code section relating to memory using a hardware transactional approach to executing code sections **[see Col. 2, lines 30-36; critical section is speculatively executed without the use of software locks]**,

where the hardware approach to executing code sections is employed to attempt to execute the code section before a software approach to locking memory is ever

employed to attempt to execute the code section, such that a first time the code section is attempted to be executed the software approach to locking memory is not employed to attempt to execute the code section prior to the hardware transactional approach being employed to attempt to execute the code section **[see Rajwar, Fig. 5, Col. 7, lines 56-67 to Col. 8, lines 1-20, and Claims 1 and 14-16; Rajwar discloses the process of Fig. 5 is implemented in hardware. Further the process begins by determining whether a lock is currently held. This determining is still part of the hardware approach, not the software approach. In the instance that it is determined that the lock is *not held*, the software approach to locking memory has ***not*** been attempted and the process then continues to execute the code using the hardware approach. This is further evidenced in claims 1 and 14-16, wherein Rajwar teaches implementing the hardware approach without ever even detecting whether a lock is held. Therefore, Rajwar explicitly teaches an embodiment that executes a code section using a hardware approach before a software approach is ever attempted.]**; and,

where the hardware transactional approach to executing code sections fails a threshold in executing the code section, executing the code section relating to the memory using a software approach to locking memory **[see Col. 3, lines 60-64; critical section re-executed a predetermined number of times. If a conflict still exists, a lock variable is acquired and used]**

2. Regarding claim 2, Rajwar and Herlihy teach the method of claim 1, further comprising executing other code sections relating to the memory using the software approach to locking memory **[see Col. 3, lines 60-64; the critical section of any code is executed using the software approach if the hardware approach fails a predetermined number of times]**.

3. Regarding claim 3, Rajwar and Herlihy teach the method of claim 1, wherein executing the code section relating to the memory using the hardware transactional approach to executing code sections comprises:

starting a transaction inclusive of the code section **[see Col. 2, lines 30-36; critical section begins execution]**; and,

conditionally executing the transaction **[see Col. 7, lines 44-50; critical section conditionally executed]**.

4. Regarding claim 4, Rajwar and Herlihy teach the method of claim 3, wherein executing the code section relating to the memory using the hardware transactional approach to executing code sections section further comprises, upon successfully completing the transaction, committing execution of the transaction to the memory to which the code section relates **[see Col. 2, lines 30-36; execution committed if no errors occur]**.

5. Regarding claims 5 and 6, Rajwar and Herlihy teach the method of claim 1, wherein the hardware transactional approach to executing code sections failing the threshold in executing the code section comprises the hardware transactional approach to executing code sections aborting execution of the code section a single time or a predetermined number of times **[see Col. 3, lines 60-64, the retry limit can be set at any number]**.

6. Regarding claim 8, Rajwar and Herlihy teach the method of claim 1, wherein the hardware transactional approach to executing code sections failing the threshold in executing the code section comprises utilizing information passed from a compiler to determine whether to utilize the software approach to locking memory to execute the code section **[see Col. 3, lines 1-5; existing compiler detects critical section]**.

7. Regarding claim 9, Rajwar and Herlihy teach the method of claim 1, wherein the hardware transactional approach to executing code sections failing the threshold in executing the code section comprises tracking a success rate of the hardware transactional approach to executing code sections in executing the code section to determine whether to utilize the software approach to locking memory to execute the code section **[see Col. 8, lines 12-15; prediction table with success rate used to determine if software approach should be used]**.

8. Regarding claim 10, Rajwar and Herlihy teach the method of claim 1, wherein executing the code section relating to the memory using the software approach to locking memory comprises:

placing a lock on the memory to which the code section relates **[see Fig 2, 30, Col. 5, lines 17-19; lock acquired]**;

executing the code section **[see Fig. 2, 44, Col. 5, lines 23-25; critical section executed]**;

committing execution of the code section to the memory as the code section is executed; and **[see Fig. 2, 44, Col. 5, lines 23-25; critical section executed, changes are committed]**,

removing the lock on the memory to which the code section relates **[see Fig. 2, 32, Col. 5, lines 24-26; lock released]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar in view of Herlihy, as applied to claims 1-6, 8-10, and 18-20 above, and in further view of McKenney (US 2002/0078284).

17. Regarding claim 7, Rajwar and Herlihy teach the method of claim 1, wherein utilization of the hardware transactional approach to executing code sections failing the threshold in executing the code section comprises using a success rate in determining whether to utilize the software approach to locking memory to execute the code section **[see above]**.

Rajwar and Herlihy do not disclose expressly that a digital filter is used as the threshold for determining whether to use the software approach.

McKenney discloses a method for dynamically selecting an optimal lock mode in a multiprocessor environment. He also discloses using a digital filter for taking measurements to determine an optimal opportunity for switching to an alternative locking mode **[see paragraphs 9 & 29]**.

Rajwar, Herlihy, and McKenney are analogous art because they are from the same field of endeavor, namely executing code relating to transactional memory.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system of Rajwar and Herlihy with the digital filter taught by McKenney.

The motivation for doing so would have been to determine the optimal opportunity for switching to an alternative locking mode **[see McKenney, paragraph 29]**.

Therefore, it would have been obvious to combine Rajwar and Herlihy with Radovic for the benefit of efficiently determining when to switch to a different locking mode to obtain the invention as specified in claim 7.

18. Regarding claim 11, Rajwar and Herlihy teach the method of claim 1 as described above.

Rajwar and Herlihy do not disclose that executing the code section relating to the memory using the software approach to locking memory comprises utilizing one of a queued lock, a non-uniform memory architecture (NUMA) lock, and a reader-writer lock.

McKenney discloses the lock mode in NUMA machines consisting of a reader-writer lock mode **[see paragraph 9; reader-writer lock]**.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system of Rajwar and Herlihy with software locking options taught by McKenney.

The motivation for doing so would have been to synchronize processes **[see paragraph 9]**.

Therefore, it would have been obvious to combine Rajwar and Herlihy with Radovic for the benefit synchronized processes, to obtain the invention as specified in claim 11.

II. RESPONSE TO APPLICANT'S ARGUMENTS

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

III. CLOSING COMMENTS

Conclusion

(a) **Status of Claims In the Application**

(i) Claims Rejected In the Application

Per the instant office action, claims 1-11 have received a fifth action on the merits and are subject of a final rejection.

(b) **Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Bertram whose telephone number is 571-270-1377. The examiner can normally be reached on Mon-Fri 9am-5:30pm ET.

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on 571-272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Bertram/
Examiner, Art Unit 2187

/Kevin L Ellis/
Acting SPE of Art Unit 2187